ABSTRACT OF THE DISCLOSURE

A memory circuit and method for reducing gate oxide stress is disclosed. A first data word is stored at a first address in a nonvolatile memory circuit 604. The first address 820 and the first data word 842 are stored in a volatile memory circuit 602. A first external address 608 is applied to the volatile memory circuit. The first external address is compared to the first address. The first data word is produced from the volatile memory circuit on a data bus 610 when the first external address matches the first address. The first data word is produced from the nonvolatile memory circuit on the data bus when the first external address does not match the first address.